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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/707,163 | 11/25/2003 | Wei-Chih Lai | 10659-US-PA | 1162 |

31561 7590 09/30/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

| EXAMINER | |
|---|---|
| CANNING, ANTHONY J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2879 | |

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/707,163 | LAI ET AL. | |
| | Examiner | Art Unit | |
| | Anthony J. Canning | 2879 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (U.S. 2002/0005696 A1).

3. As to claim 1, Yamazaki et al. disclose an organic light-emitting display (OLED), comprising: a plurality of power line sets isolated from each other (see Fig. 5, items $V_n$, $V_1$, and $V_2$; paragraph 0016), wherein each power line set is coupled to a plurality of secondary power lines (see Fig. 5, items $V_{b1}$-$V_{b3}$; paragraph 0016); and a plurality of voltage terminals (see Fig. 5, where the secondary power lines connect with the power line that is connected to the external power supply, item 116), wherein each voltage terminal is coupled to a center of a power line set, and the voltage terminals are coupled to a power supply (see Fig. 5, item 116; paragraph 0016, the external switching is a power supply), wherein an electric current resulting from a voltage applied to each power line set passes through the secondary power lines into a plurality of corresponding pixels in the organic light-emitting display (see Fig. 5, item 104; paragraph 0017).

4. As to claim 2, Yamazaki et al. disclose the OLED of claim 1. Yamazaki et al. further disclose that the pixels are arranged in a pixel array (see Fig. 5, item 104; paragraph 0017).

5. As to claim 3, Yamazaki et al. disclose the OLED of claim 1. Yamazaki et al. further disclose that each pixel comprises: a switching transistor (see Fig. 6, item 1701; paragraph 0017) having a first drain terminal (paragraph 0018), a first gate terminal (see Fig. 6, item 1705; paragraph 0018) and a first source terminal (paragraph 0018), wherein the first drain terminal is coupled to a data line and the first gate terminal is coupled to a scan line (paragraph 0018); a driving transistor having a second drain terminal (see Fig. 6, item 1702; paragraph 0017), a second gate terminal and a second source terminal, wherein the second gate terminal is coupled to the first source terminal and the second source terminal is connected to ground (see Fig. 8, item 1923; paragraph 0269); a storage capacitor having a first terminal and a second terminal (see Fig. 6, items, wherein the first terminal is coupled to the first source terminal and the second gate terminal and the second terminal is connected to ground and the second source terminal (see Fig. 5, the lines that 1704 is connected to); and a light-emitting device having an anode and a cathode, wherein the anode is coupled to one of the secondary power lines and the cathode is coupled the second drain terminal paragraph 0020).

6. As to claim 4, Yamazaki et al. disclose the OLED of claim 3. Yamazaki et al. further disclose that the switching transistor and the driving transistor comprise thin film transistors (paragraph 0018).

7. As to claim 5, Yamazaki et al. disclose the OLED of claim 3. Yamazaki et al. further disclose that the light-emitting device comprises an organic light-emitting diode (paragraph 0005).

8. As to claim 6, Yamazaki et al. disclose the OLED of claim 3. Yamazaki et al. further disclose that the light-emitting device comprises a polymer light-emitting diode (paragraph 0186).

9. As to claim 7, Yamazaki et al. disclose an organic light-emitting display (OLED), comprising: a plurality of power line sets isolated from one another (see Fig. 5, items $V_n$, $V_1$, and $V_2$; paragraph 0016), wherein each power line set is coupled to a plurality of secondary power lines (see Fig. 5, items $V_{b1}$-$V_{b3}$; paragraph 0016); and a plurality of voltage terminals (see Fig. 5, where the secondary power lines connect with the power line that is connected to the external power supply, item 116), wherein each voltage terminal is coupled to a power line set, and the voltage terminals are coupled through a conductive material medium to a power supply (see Fig. 5, item 116; paragraph 0016, the external switching is a power supply, if the medium is not conductive then current could not be drawn from the power supply into the device); wherein an electric current resulting from a voltage applied to each power line passes through the secondary power lines into a plurality of corresponding pixels in the organic light-emitting display (paragraph 0219).

10. As to claim 8, Yamazaki et al. disclose the OLED of claim 7. Yamazaki et al. further disclose that the pixels are arranged in a pixel array (see Fig. 5, item 104; paragraph 0017).

11. As to claim 9, Yamazaki et al. disclose the OLED of claim 7. Yamazaki et al. further disclose that each pixel comprises: a switching transistor (see Fig. 6, item 1701; paragraph 0017) having a first drain terminal (paragraph 0018), a first gate terminal (see Fig. 6, item 1705; paragraph 0018) and a first source terminal (paragraph 0018), wherein the first drain terminal is coupled to a data line and the first gate terminal is coupled to a scan line (paragraph 0018); a

driving transistor having a second drain terminal (see Fig. 6, item 1702; paragraph 0017), a second gate terminal and a second source terminal, wherein the second gate terminal is coupled to the first source terminal and the second source terminal is connected to ground (see Fig. 8, item 1923; paragraph 0269); a storage capacitor having a first terminal and a second terminal (see Fig. 6, items, wherein the first terminal is coupled to the first source terminal and the second gate terminal and the second terminal is connected to ground and the second source terminal (see Fig. 5, the lines that 1704 is connected to); and a light-emitting device having an anode and a cathode, wherein the anode is coupled to one of the secondary power lines and the cathode is coupled the second drain terminal paragraph 0020).

12. As to claim 10, Yamazaki et al. disclose the OLED of claim 9. Yamazaki et al. further disclose that the switching transistor and the driving transistor comprise thin film transistors (paragraph 0018).

13. As to claim 11, Yamazaki et al. disclose the OLED of claim 9. Yamazaki et al. further disclose that the light-emitting device comprises an organic light-emitting diode (paragraph 0005).

14. As to claim 12, Yamazaki et al. disclose the OLED of claim 9. Yamazaki et al. further disclose that the light-emitting device comprises a polymer light-emitting diode (paragraph 0186).

***Contact Information***

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Canning whose telephone number is (571)-272-2486. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh D. Patel can be reached on (571)-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anthony Canning
22 September 2005

ASHOK PATEL
PRIMARY EXAMINER